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Proton-induced single-event effect and influence of annealing on multiple feature size NAND flash memory

Cong Peng[1], Wei Chen[1,2], Yinhong Luo[2*], Fengqi Zhang[2], Xiaobin Tang[1*], Xiaoqiang Guo[2], Jiangkun Sheng[2], Lili Ding[2], and Zibo Wang[2]

[1]*Department of Nuclear Science and Technology, Nanjing University of Aeronautics and Astronautics, Nanjing 210106, People's Republic of China*
[2]*State Key Laboratory of Intense Pulsed Radiation Simulation and Effect, Northwest Institute of Nuclear Technology, Xi'an 710024, People's Republic of China*

[*]E-mail: luoyinhong@nint.ac.cn; tangxiaobin@nuaa.edu.cn

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The proton-induced single-event effect sensitivity of multiple feature size NAND flash memories has been studied. The single-event upset cross section of memories was obtained as a function of feature size, and the cross section of device increases significantly with increasing integration. Monitoring of the proton-irradiated devices for up to 2 months indicates that the retention errors of devices due to reduced insulating properties of the tunnel oxide layer are more critical than error annealing due to the annealing of the trapped charge. During the dynamic test, a large number of semipermanent and regular data "stuck bit" errors were captured, which disappeared after a few days of annealing. Micro-dose effect, which occurred in the external control circuit of NAND flash by proton-produced secondary particles, is considered responsible to the "stuck bit" errors.

1. Introduction

NAND flash memory plays a critical role in the nonvolatile semiconductor memory commercial market due to its large capacity, low power consumption and cost. Commercial flash memory is also attractive for space applications and has been used as a data storage device in many space missions.[1,2] However, the space radiation environment poses a radiation risk to electronic memory devices,[3–5] which represents a considerable hidden danger to the successful completion of the space mission. As a result, evaluating the radiation sensitivity of NAND flash memory is critical to its space applications.

The data storage cell of NAND flash memory is the floating gate (FG) MOS transistor, and the storage cell can be divided into single-level cell (SLC) and multilevel cell (MLC). In the past, the radiation effect of flash memory was focused on the total ionizing dose, especially the thick-oxide charge pump circuit in the external control circuit.[6] With the rapid development of CMOS technology, the feature size of devices was gradually decreased. FG arrays produce a large amount of single-event upsets (SEUs) after being exposed to ionizing radiation, and the error cross section exceeds that of the external circuit. NAND flash memories then become sensitive to single-event effects (SEEs).[7,8] When devices generate SEUs, errors are also annealed at the same time. Ignoring the annealing effect may cause an overestimation or underestimation on the number of errors.

Over the few past decades, researchers have conducted extensive experimental studies on the SEE of each generation of NAND flash memories by using heavy ions.[9–17] Single-event damage of multiple feature size NAND flash memories by heavy ions with different linear energy transfers (LETs) was reported,[11–14] and the change in SEU cross section with the variation in device feature size was observed. The variation of device errors with time after heavy ion irradiation was studied, and the physical mechanism of the FG array's error change during long-time annealing was analyzed.[15–17] In addition to the irradiation response induced by heavy ions, the proton irradiation response of NAND flash memories has also been studied by some researchers.[18–20] The Monte Carlo simulation method was used to simulate the process of proton irradiation devices. The LET value distribution of secondary particles generated by proton irradiation was calculated.[18,19] In addition, an exploratory experiment was conducted on the SEE sensitivity of low-energy proton-induced devices. High-scaling devices are more sensitive to low-energy protons than to high-energy protons.[20] In summary, no reports are available on the proton-induced SEE of SLC and MLC devices with a series of multiple feature size of the same manufacturer's technology and the error response to time variation after proton irradiation.

This work aims to study the proton-induced SEE on flash devices of multiple feature sizes down to 16 nm, and the variation in data errors with time after proton irradiation. The paper is organized as follows. First, the features of the samples under investigation and the experimental details are presented. Then, the results on FG errors induced by proton irradiation are shown and analyzed, wherein we discuss the variation mechanism of device errors as time progresses after proton irradiation. Finally, the response of the external circuits of devices under test (DUTs) after the proton dynamic test is analyzed.

2. Devices and experimental details

In this work, all DUTs were manufactured by micron technology and packaged in 48-pin TSOP. The DUT information is shown in Table I.

The proton irradiation experiment was carried out at the 100 MeV proton cyclotron at the China Institute of Atomic Energy (CIAE), and the proton energy was adjusted to 50–90 MeV by aluminum foils. The static unbiased test was performed on all devices by the self-developed flash memory test system. Only some devices were dynamically tested due to the time limit of proton beam. In order to have more visibility on proton-induced SEE, error correcting code was not applied in test devices.

2.1. Static unbiased test

The normal incidence proton irradiation test was performed on all unbiased devices to study the radiation sensitivity of

Table I. Parameter information of micron NAND flash memories used in test.

Part number	Date code	Feature size (nm)	Capacity (Gb)
29F1G08AAC	0940 1-2	120	1
29F8G08AAA	0918 1-2	51	8
29F32G08ABAAA	1329 2-2	25	32
29F32G08CBACA (MLC)	1244-2-7	25	32
29F64G08CBEFB (MLC)	1538 2-2	16	64

Table II. Static unbiased test proton beams used at CIAE.

Energy (MeV)	LET in Si (MeV cm^2 mg^{-1})	Range in Si (mm)	Fluence (p cm^{-2})
50	0.0099	12.18	5×10^9
90	0.0063	34.56	5×10^9

Table III. Dynamic test proton beams used at CIAE.

Energy (MeV)	LET in Si (MeV cm^2 mg^{-1})	Range in Si (mm)	Fluence (p cm^{-2})
50	0.0099	12.18	5.7×10^9
70	0.0076	22.16	2.5×10^9

the device FG array. The device under test was programmed with checkerboard "55" before irradiation, the proton beam parameters are shown in Table II. All test samples were to be readback at room temperature after 3 d, and the error messages were recorded. The samples remained unbiased in the air at room temperature, multiple data readbacks were implemented, and error changes were recorded over the next 2 months.

2.2. Dynamic test

The normal incidence proton irradiation was performed on 1, 8, and 32 G SLC DUTs to study the external circuit radiation sensitivity of devices. Figure 1 shows the system diagram of dynamic test. DUTs were filled with checkerboard "55" and biased at 3.3 V. The proton beam parameters are shown in Table III.

Given that it takes too much time to readback all blocks data, before the dynamic test, only a part of the blocks of the DUTs were initialized with checkerboard "55". During the irradiation process, the selected 10 blocks that are not initialized and a continuous erase–write–read cycles was performed (with checkerboard "55"). The dynamic test data and functional errors were recorded. When protons were accumulated to the required total fluence, data readback was performed on all blocks that were initialized with checkerboard "55," and the error information was counted. A dynamic test was performed on the next device, and the abovementioned process was repeated until all devices were tested.

3. Results and discussion

3.1. Static unbiased test

3.1.1. Effect of devices by proton irradiation. Data readback was performed on all devices on the third day after proton irradiation. The functions of DUTs are normal without any destructive events. Figure 2 shows the SEU cross section of DUTs with different feature sizes under static proton irradiation. A few inherent errors in MLC devices are deducted when their SEU cross sections are calculated.

With the scaling of technology, the SEU cross section of DUTs shows a significant upward trend under the proton irradiation. With the decrease of the feature size, the sensitive volume of the FG cell array and the amount of sensitive charge required for SEU also decrease.[19,21] Proton irradiation produces ionization in a particular track area. There are more substantial cells in the track area due to the smaller feature size, and numerous cells will collect sufficient charge to generate considerable SEUs. Therefore, devices of small feature sizes are highly sensitive to proton-induced SEUs. However, the SEU cross section of the 120 nm device (1 G) is higher than that of the 51 nm device (8 G) at 90 MeV proton irradiation. The charges generated by the 90 MeV proton is high enough to cause SEU on 1 G SLC and 8 G SLC. Compared with 8 G SLC, the 1 G SLC cell has a larger sensitive area, resulting in a higher SEU cross section. The scaling effect is effective below a certain feature size.[22] The difference in device SEU cross section caused by 50 and 90 MeV protons is small. This result indicates that device SEU cross section is saturated at 50 MeV proton irradiation, which is similar to the results of previous studies.[20]

The 32 G SLC and 32 G MLC devices exhibit the same 25 nm feature. Under the proton irradiation, the SEU cross section of the MLC devices is one order of magnitude higher than that of the SLC devices. Compared with SLC, MLC has more threshold voltage states and less reference voltage interval. MLC read margins are significantly lower than in SLC devices, which leads to the reduction in fault tolerance.[7]

Upsets of devices under 50 and 90 MeV proton irradiation are counted, and the SEU difference of devices at two energies is found to be small. All SLC device errors are "0 → 1" upsets, whereas MLC devices present "0 → 1" and "1 → 0" upsets, as shown in Fig. 3. For SLC devices, proton

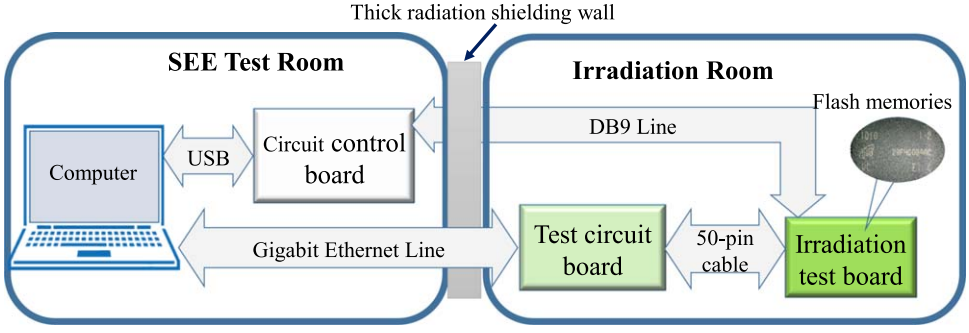


Fig. 1. (Color online) Dynamic test system diagram of NAND flash memories.

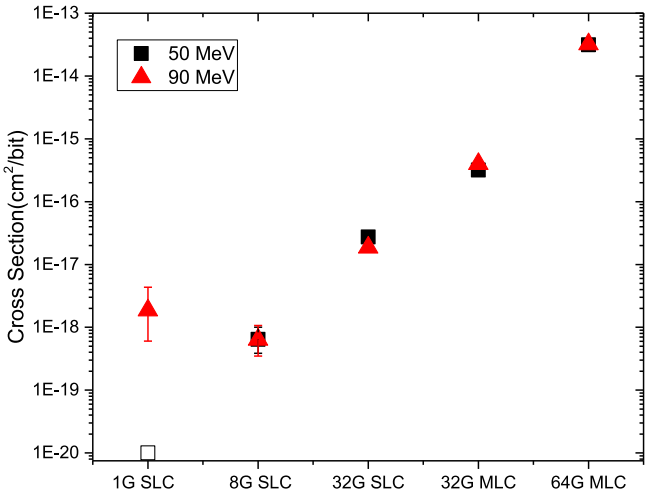


Fig. 2. (Color online) SEU cross sections of DUTs under static proton irradiation. Open symbols indicate "No errors up on this device" (Initialization with checkerboard "55").

irradiation causes charge leakage and loss in FG cells, which leads to the "0 → 1" upset. Proton irradiation does not allow a large number of charges to enter the FG (this would need to be achieved by Fowler–Nordheim tunneling or hot electron injection at high gate-substrate voltage).[23,24] Thus, the "1 → 0" upset does not occur in the SLC devices. MLC devices have used multipage cell architecture. Two-bit data written to the same FG cell are allocated to two shared pages of the least and most significant bit pages. Proton-induced charge leakage and disturbance may cause the FG cell data to jump in various states, and a large number of "0 → 1" and "1 → 0" upsets to occur.

Logical address mapping was performed on the devices' error data to obtain the error logical location map. Figures 4 and 5 show the maps of DUTs under proton irradiation. As feature sizes decrease, device error densities increase. The locations of DUT data errors are random distributed, which indicates that SEE occurs in the FG array region of flash devices. It is only when radiation damage occurs in the external circuit that DUTs may suffer from destructive read/write function failure or large-area read errors.[6]

3.1.2. Annealing effect. The proton-induced DUT errors were monitored for up to 2 months to study the variation in FG errors as time progressed after proton irradiation. All test data were normalized using the error data of the first test, as shown in Fig. 6. Errors of the 50 MeV proton-irradiated 8 G SLC device and 90 MeV proton-irradiated 32 G SLC device were partially annealed from the third day to the eleventh day, and the number of errors decreased as time increased. After 11 d, the device errors continued to increase over time. In addition to these devices, the errors of other proton-irradiated devices increased as time increased.

Some explanations have been proposed on how the mechanism of NAND flash generates errors. For example, the transient carrier current of tunnel oxide or the transient conductive path formed by ion incidence in the FG cell will induce instantaneous leakage loss of FG charges,[25,26] and the threshold voltage shift is $\Delta V_{T,L1}$. After ionizing irradiation, FG tunnel oxide generates a large number of trap defects to form a multi-trap-assisted conductive channel, which produces a permanent charge leakage path.[27–29] FG charges are then released slowly, and the threshold voltage shift is $\Delta V_{T,L2}$. Tunnel oxide impurity traps generated by ion irradiation trap the charge generated by irradiation,[8,16] which leads to the threshold voltage shift of $\Delta V_{T,C}$. The total threshold voltage shift is ΔV_T

$$\Delta V_T = \Delta V_{T,L} + \Delta V_{T,C} = \Delta V_{T,L1} + \Delta V_{T,L2} + \Delta V_{T,C}. \quad (1)$$

After proton irradiation, the charges of some FG array cells are instantaneously lost, and their threshold voltage V_{th} has a large shift, $\Delta V_{T,L1}$. When V_{th} crosses through the read voltage, devices generate data errors. These errors can only be eliminated by rewriting. The multi-trap-assisted conductive channel causes a slow cells charges loss, and $\Delta V_{T,L2}$ gradually increases as time progresses, which increases retention errors.[29] The charge is trapped by the FG tunnel oxide impurity trap, which causes threshold voltage V_{th} to shift $\Delta V_{T,C}$. However, $\Delta V_{T,C}$ will gradually anneal over time. If V_{th} recovers above the read voltage after annealing, then the error will disappear, as shown in Fig. 7.

After proton irradiation, the variation in device errors over time is the result of competition between two mechanisms of

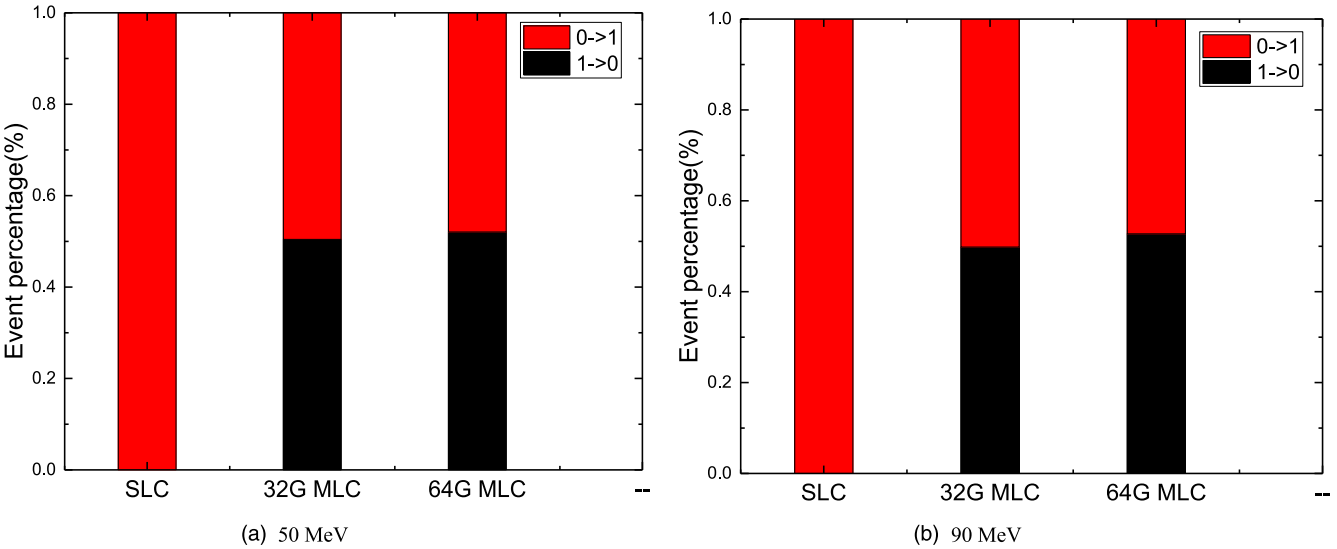
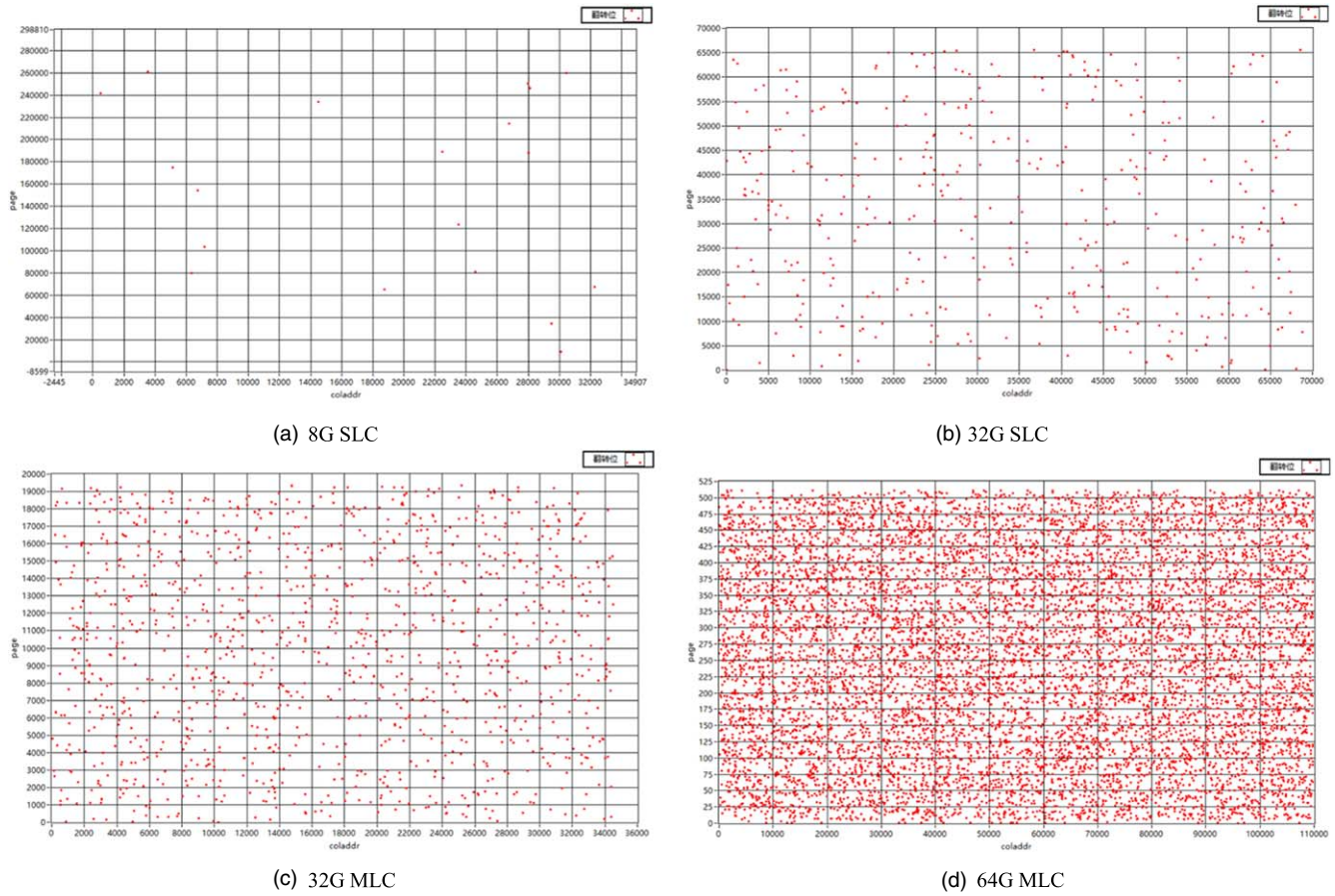


Fig. 3. (Color online) Percentages of "0 → 1" upsets and "1 → 0" upsets in DUTs under 50 MeV (a) and 90 MeV (b) proton irradiation.



(a) 8G SLC (b) 32G SLC

(c) 32G MLC (d) 64G MLC

Fig. 4. (Color online) SEU logical location maps of DUTs after 50 MeV proton irradiation in static unbiased test. (a) 8 G SLC, (b) 32 G SLC, (c) 32 G MLC, (d) 64 G MLC.

error annealing and retention error generation. The errors of the 50 MeV proton-irradiated 8 G SLC device and the 90 MeV proton-irradiated 32 G SLC device anneal partially from the third day to the eleventh day. Then, the devices mainly generate retention errors. All other proton-irradiated devices generate retention errors constantly. The competitive mechanism allows the error number to increase or decrease over time. All tests show that, after proton irradiation, device retention errors due to the insulating property degradation of tunnel oxides are more critical than the device error annealing.

3.2. Dynamic test

The devices used in the dynamic test were three types of SLC NAND flash memories. The proton test results show that no functional failure is detected on all devices. During the 70 MeV proton dynamic test of 8 and 32 G devices, the device generated many anomalous "0 → 1" and "1 → 0" upsets in dynamic erase–write–read cycles. After the 70 MeV proton irradiation, data readback was performed on blocks that were initialized with checkerboard "55" in the 8 and 32 G devices. Considerable "0 → 1" and "1 → 0" upsets were also detected. Finally, the erase–write–read operation was performed on devices after the test system was powered back on, and these error upsets did not disappear.

The SEU logical location maps for the 70 MeV proton dynamic test are shown in Fig. 8. Except for a small number of random distributed "0 → 1" upsets, many upsets appear in some fixed positions of a large number of pages, as shown in the red lines of Figs. 8(a) and 8(b). This result shows that, in addition to the FG array region, radiation damage also occurs in external circuits of devices at the same time. These fixed bit errors caused by external circuit errors are called "stuck bit" errors.

On the third day after the dynamic test, the erase–write–read operation was performed (write to checkerboard "55") on all DUTs, and all "stuck bit" errors in the 8 and 32 G devices disappeared. The dynamic test results show that proton irradiation can produce radiation effects in the FG array region and in external circuits of devices. The radiation effect of the FG array region is represented by "0 → 1" errors, in which the logical positions are random distributed. The radiation effect of the external circuit is represented by numerous "stuck bit" errors. These errors appear on the fixed position of a large number of pages and cannot be corrected by the erase–write–read operation in a short time. After DUTs leave the irradiation environment for a long period of annealing, "stuck bit" errors can be eliminated.

Under proton irradiation, protons interact with the materials of high-scaling devices to produce high-LET secondary particles. When secondary particles deposit energy in the FG array region, the devices will generate SEU errors with a random distribution of logical positions. When secondary particles impinge on external circuits, such as decoding circuits, these high-LET secondary particles may strike sensitive areas of circuit-specific thick-oxide components. These particles can deposit a sufficient ionizing dose and produce local micro-dose effects on the devices.[30–32] When the local micro-dose accumulates beyond the error threshold,

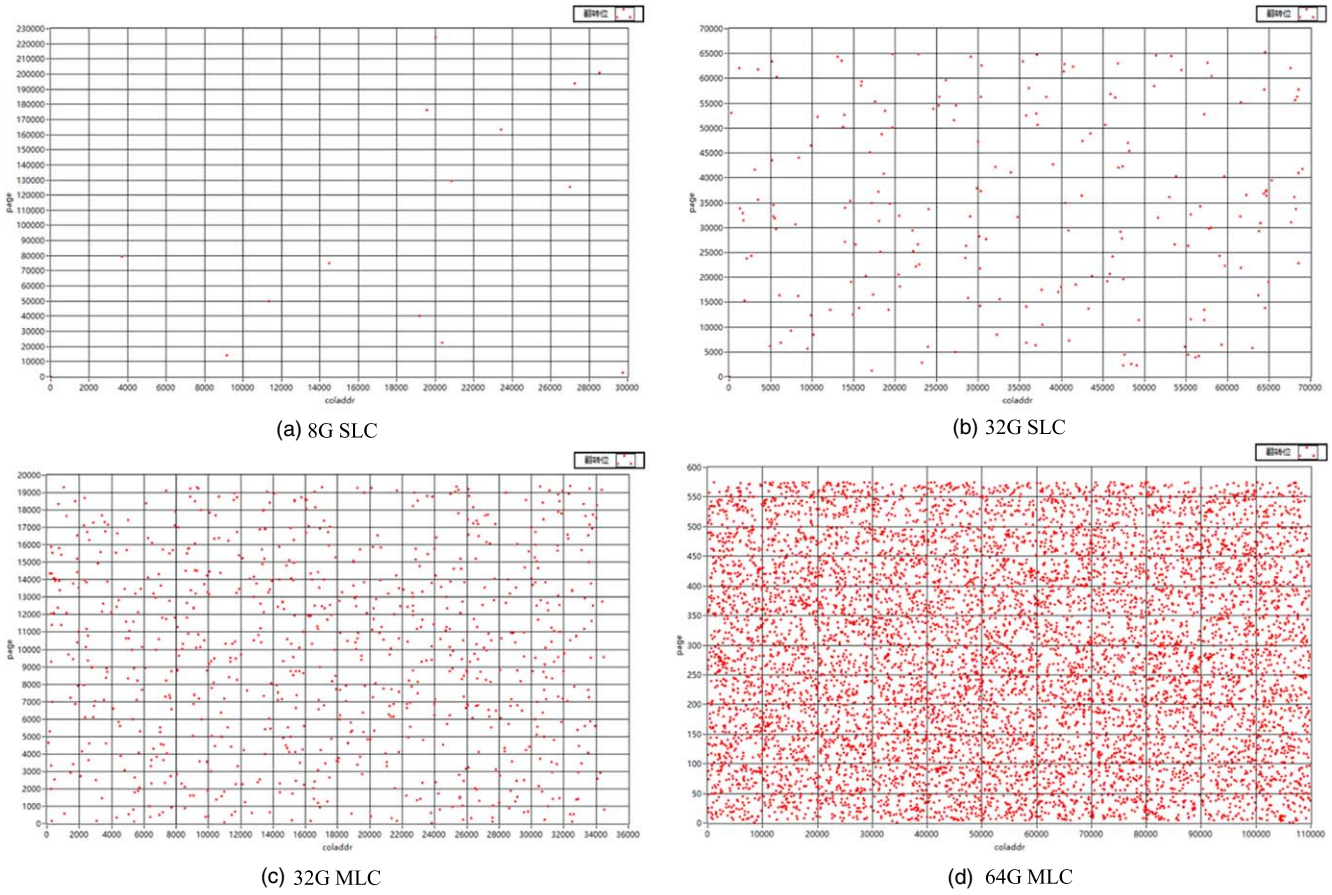


Fig. 5. (Color online) SEU logical location maps of DUTs after 90 MeV proton irradiation in static unbiased test. (a) 8 G SLC, (b) 32 G SLC, (c) 32 G MLC, (d) 64 G MLC.

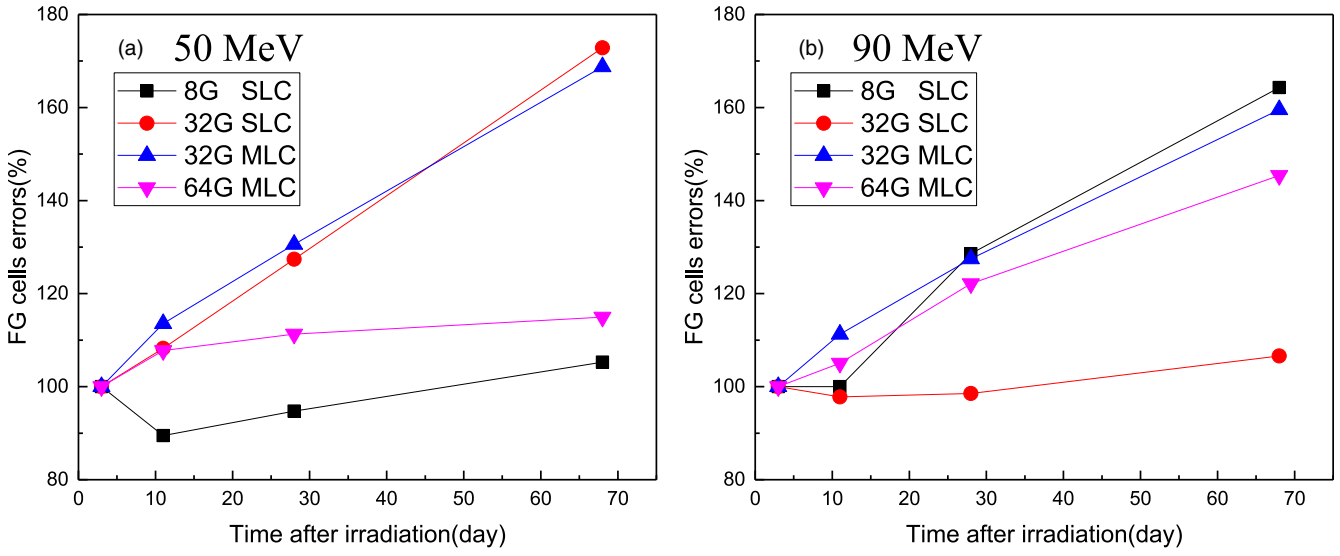


Fig. 6. (Color online) DUT error changes within 68 d after 50 MeV (a) and 90 MeV (b) proton irradiation.

the transistor cannot be switched on normally. The corresponding high and low voltages cannot be supplied to the matched word line. Eventually, the data read from several logical bits of a large number of pages are fixed "0" or "1". Considerable "stuck bit" upsets occur, which are confused with the data upsets that occur in the FG array region. These "stuck bit" errors cannot be eliminated by the erase–write operation or power cycle of the test system. The devices will eventually return to normal only after the micro-dose has gradually annealed away from the radiation environment.

4. Conclusions

This work studied the proton-induced SEE sensitivity of NAND flash memories with multiple feature sizes down to 16 nm nodes. The experimental results show that the SEU cross section of NAND flash memories has a significant upward trend with the decrease in device feature size. MLC devices are more sensitive to proton-induced SEE than SLC devices. All SEU errors in the static test are random distributed, which indicates that the device SEE occurs in the FG region. Two-month error

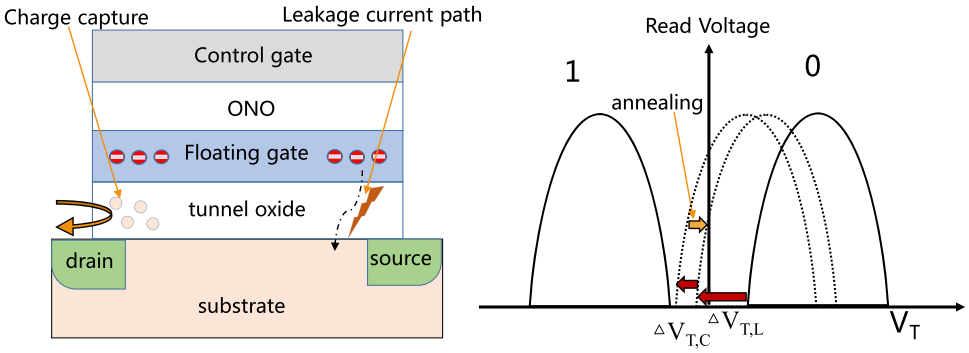
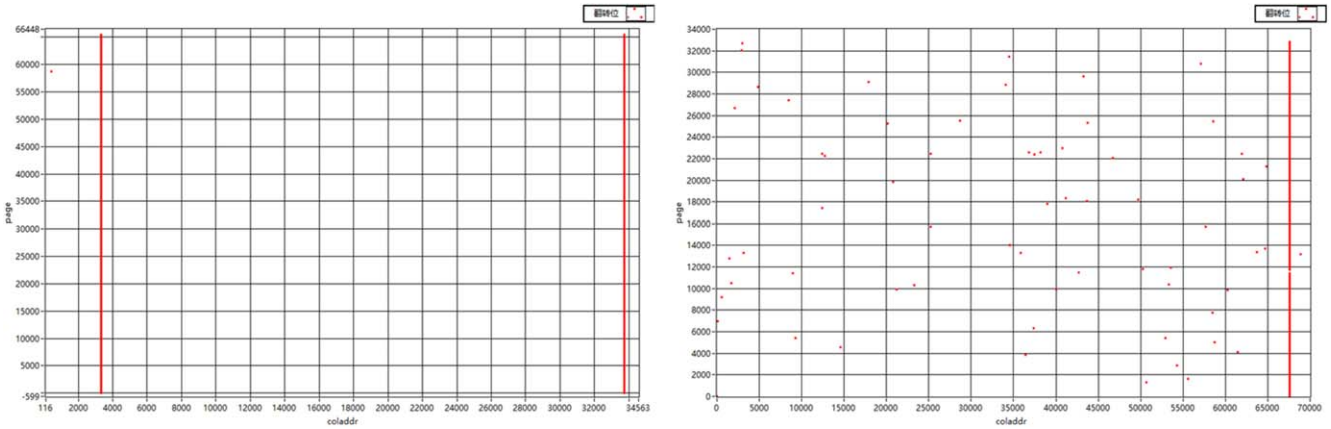


Fig. 7. (Color online) Tunnel oxide leakage current channel and trap defects in FG and the resulting threshold voltage change.



(a) 8G SLC (b) 32 G SLC

Fig. 8. (Color online) SEU logical location maps of 8 G (a) and 32 G (b) devices under dynamic proton irradiation at 70 MeV.

monitoring of proton-irradiated DUTs shows that, after proton irradiation, NAND flash memories have two processes of error annealing and retention error generation. The change of the error number is the result of competition between the two mechanisms. Compared with error annealing, the generation of device retention errors is dominant.

External logic circuits still require components with a thick gate oxide due to the functional circuit requirements of the flash memory. During proton irradiation, the micro-dose effect of protons in the local external circuit leads to large-scale regular "stuck bit" errors, and devices need to be annealed for a long-time to return to normal. Therefore, the effects of secondary particles generated by protons on the external circuits of devices must be considered. Higher- or lower-energy proton beam currents will be used in our future work, the multiple modes of functional interrupt of devices under high-energy proton irradiation and the SEE sensitivity differences of devices under low-energy proton irradiation needs to be further studied.

Acknowledgments

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