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Proton-induced single-event effects on 28 nm Kintex-7 FPGA

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ABSTRACT

Proton experiments were performed on Kintex-7 XC7K70T field programmable gate array by using a self-developed test system at EN tandem accelerator in Peking University. The single-event upset and multiple-bit upsets induced by low-energy proton were presented, and a cross section peak under the low-energy protons was tested. Also, the experiments under high-energy protons were performed on the proton cyclotron accelerator in the China Institute of Atomic Energy, cross sections of some blocks in FPGA were obtained. Data of low-energy and high-energy experiments showed that the LET threshold of some resources were different. Results suggest that the low-energy proton-induced single event effect must be considered.

1. Introduction

Field programmable gate arrays (FPGAs) have received extensive attention from researchers in various fields because of advantages such as programmability, low-price, and high-performance. Commercial FPGAs have been increasingly used in satellites and other spacecrafts. However, the aerospace environment brings severe challenge, due to charged particles that can induce single-event effects (SEE) easily in the resources of SRAM-based FPGAs, such as configurable logic blocks (CLBs), and block-rams (BRAMs) [1]. As a result, it's necessary to evaluate the SEE sensitivities of FPGAs when they are applied to aerospace engineering. Considering that single-event upset (SEU) is the most common phenomenon of SEE, the evaluation of SEU on FPGAs is crucial to take targeted methods in reinforcing the device.

With the scaling of technology, the feature size of FPGAs is reduced to 28 nm or even smaller, the amount of resources and performance per watt in FPGAs has remarkably improved. SEU occurs when a particle flips a single memory cell, and multiple-bit upsets (MBUs) happen in the FPGA when the particle flips several bits in the same frame. The effect of the reduction in feature size is complicated: the reduction in feature size leads to a reduction of the distance between the cells. Then a particle could affect several cells, therefore, the probability of MBU on FPGAs becomes higher. Moreover, the LET threshold that causes flipping is also lowered, which cause the SEU-sensitivity increased due to the feature size reduction [2].

Considerable studies on FPGA with a feature size of 28 nm or even smaller have been conducted. A recent work [3] described the different resources SEU cross section in 28 nm FPGA under heavy ions, such as BRAM, and CLB. References [4, 5] compared the electron induced SEU cross sections of 45-nm, 28-nm and 20 nm FPGAs, their results showed that the sensitivity increased with the reduction in feature size. These investigations demonstrate that the radiation effects of 28 nm FPGA are more susceptible to SEE than the previous FPGAs. Given that more protons are available in aerospace than heavy ions (e.g. van Allen belt), investigating proton-induced SEU on FPGAs is important. Till now, most of the current studies have focused on the SEU on FPGAs induced by high-energy protons, heavy ions, or other particles. However, since Rodbell [6] discovered that low-energy protons could cause upsets due to direct ionization in SRAM, more attention has been paid on this research topic. Given that the feature size decreased, MBUs can also be generated under the proton in SRAM [7]. However, for SRAM-based FPGA, studies on low-energy proton-induced SEU are limited. Therefore, the SEUs of FPGA under low-energy protons are worth to be investigated.

In this work, a multifunctional test platform for 28-nm FPGA radiation test was developed. Then the SEE experiments were performed on SEU on 28 nm SRAM-based FPGA with low-energy protons. Meanwhile, MBU and SBU were classified using a mathematical method. High-energy protons experiments were also carried out to test the SEU on 28 nm FPGA. In the end, the results were analyzed and compared.

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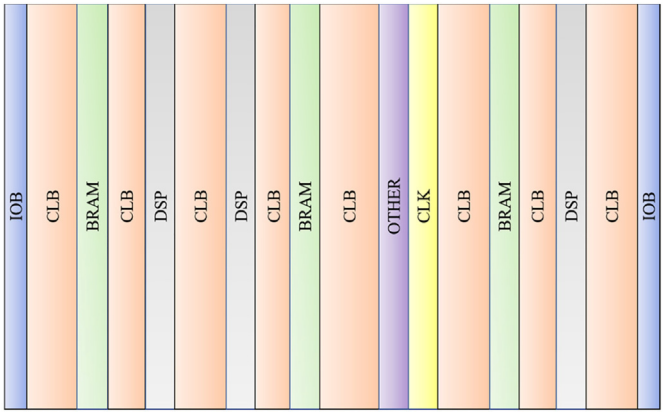

Fig. 1. Resource columns in one of the rows of XC7K70T logical layout.

2. Test platform and experimental setup

2.1. Test device

The device under test (DUT) was Kintex-7 XC7K70T FPGA from Xilinx, of a commercial 28 nm planar CMOS technology. Kintex-7 FPGAs offer several types of resources such as CLB, BRAM, DSP, and other supplemental functional features. There are the least resources in XC7K70T of Kintex-7 family [8], but it has a variety of resources, and it's also convenient to realize the frames. The frame is the basic segment of the bitstream. In fact, configurable resources in FPGA are always configured by loading bitstreams into the configuration memory based on SRAM cells. A frame in 7series FPGA, including Kintex-7 family, is composed of 3232 bits [9]. The logical layout of XC7K70T can be easily determined with the design tool. Moreover, there are 4 rows in the chip and Fig. 1 shows the resource columns in one of these rows.

Using partial reconfiguration to determine the frames correspond to the resource is easy. Thus, with the logical layout obtained from Xilinx design tools such as Fig. 1, it can be inferred that a CLB or I/O block (IOB) column occupies 36 frames, whereas those for BRAM or DSP occupies 28 frames. Noted that there are a lot of corresponding interconnected resources around CLB, BRAM, DSP, IOB and other resources. The relationship between the resources and the number of frames in bitstream was obtained using partial reconfiguration. However, the meaning of each bit in the bitstream could not be understood accurately. In other words, the resources and the corresponding resources cannot be separated accurately.

2.2. Test platform

A corresponding platform was developed to evaluate the SEU characters of 28 nm FPGA. This platform was divided into hardware and software parts. In detail, the hardware was composed of the power board, control board and irradiation board, whereas the software part was generated by LabVIEW, and the software was used to control the computer hardware. There are two same chips on the irradiation board. One is the DUT and the other is the golden. The golden one and the DUT operate at the same environment, voltage and test circuits. And their output will be compared in real time. The power board and control board both need 12 V DC power supply. Both of them are controlled by Spartan-6, the corresponding bitstreams are configurated from the flash memory. The 7 series FPGAs have several configuration interfaces and the Slave SelectMap mode was used in this platform. The computer software issues the commands into the control and power boards, and then the readback-data are extracted from DUT through the control board and displayed on the screen. Actually, the readback-data are the flipped bits or function errors. Then, the bitstream and readback file which generated beforehand should be downloaded from the computer into the flash memories on the control board. Then the DUT and the golden can be programmed with the bitstream in the flash memories. Subsequently, the test-vector should be loaded to obtain the initial accurate data which are used to test the functional failure of the DUT as expectations before irradiating. The time interval of each readback can be adjusted, and the readback data will be stored in the preset storage path (Fig. 2).

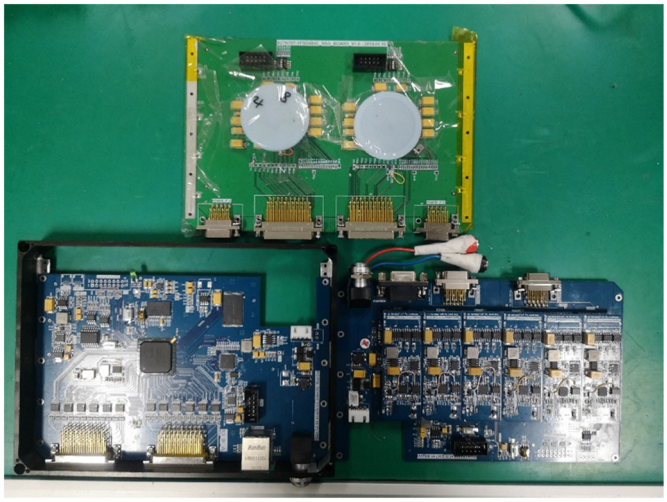

Fig. 2. Control, power and irradiation boards of the FPGA test system.

2.3. Experimental details

2.3.1. Low-energy proton experiment

The low-energy proton tests were performed at Beijing proton cyclotron accelerator in China Institute of Atomic Energy (CIAE) and EN tandem accelerator in Peking University. The EN tandem accelerator provides a range from 1.2 MeV to 10 MeV protons and the chamber vacuum is 10^{-3} Pa.

In this work 5 MeV protons were selected as the initial energy from the EN tandem accelerator. The experiments were performed in a vacuum because low-energy protons have short ranges. Noted that the DUT is a flip chip, and the substrate thickness obtained by the longitudinal cutting of the DUT was approximately 780 μm. However, the range of 5 MeV protons is roughly equal to and 216 μm in silicon calculated by using TRIM. As a result, the DUT was thinned before the experiment. At first, the thickness of the substrate was supposed to set at 100 μm after being thinned. However, we were uncertain on the actual thickness of the thinned chip due to the error in grinding, therefore, the true thickness will be calculated before the analyzation at Section 4.1. Moreover, the aluminum foils were used to get the protons whose energy are lower than the initial energy. Aluminum foil with different thickness was selected to reduce the proton energy which are listed in Table 1. The range in silicon corresponding to proton energy was calculated by using TRIM are also listed.

Different energy of protons should be obtained to test the SEU of FPGA in the low-energy proton experiment. To avoid replacing the aluminum foil by frequently opening of the vacuum chamber, which is a waste of time, a turntable with a stepper motor was used to clamp six aluminum foils. The required aluminum foil was selected on the basis of the stepper motor rotation. The irradiation board was fixed on the designed bracket. To simplify the measurement process, the memories of the DUT and the golden chip were configured with the content of 55AA in hexadecimal. Fig. 3 presents the low-energy proton experimental device.

2.3.2. High-energy proton experiment

In this experiment, 50 and 90 MeV protons were provided by proton

Table 1
Detailed information of the proton energy and range in silicon after 5 MeV proton passed through aluminum foil.

No.	Thickness of aluminum foil/ μm	Proton energy/ MeV	Range in silicon/μm
1	0	5.00	215.93
2	100	3.21	102.91
3	110	2.99	91.54
4	115	2.88	86.07
5	121	2.74	79.33
6	124	2.66	75.58
7	127	2.59	72.36
8	130	2.51	68.76
9	135	2.39	63.51

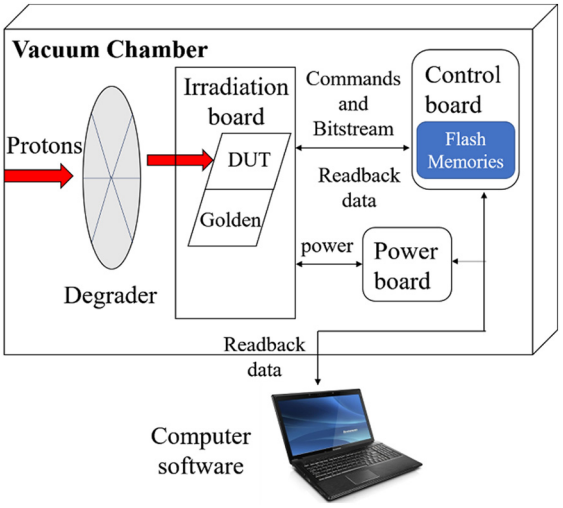

Fig. 3. Experimental device of low energy proton test in the vacuum chamber.

cyclotron, and the same user circuit was configured into the DUT and the golden. The range of the protons with the energy more than 50 MeV energy was significantly higher than 780 μm. Hence, thinning the DUT substrate was unnecessary. The experiment was carried out in air and the spot beam area of the protons was 5 × 5 cm^2. And the devices placement in high-energy proton experiment is similar to Fig. 3 except for the vacuum chamber.

3. Classification method for SBUs and MBUs

As mentioned above, MBU is defined as an event with more than one upset in the same configuration frame induced by one particle. Therefore, the readback bitstream from DUT should be compared with the golden device in real time. Whether the upsets happened in CRAM or BRAM can be determined according to the bit positions in the entire bitstream.

The method used to classify the MBUs was proposed in references [10–13]. We selected a low flux in the low-energy proton test, resulting in a small number of upsets each run. In this case, the classification work was remarkably simplified. The MBU extraction process can be divided into several steps: First the upset data should be collected according to the logical address. Second the corresponding coordinates could be set up, of which the X-dimension was defined as the number of DUT frames, and the Y-dimension indicated the number of the bits in a frame. Finally, the MBUs could be extracted from the preset coordinate.

True MBUs are not generated from different particles. Furthermore, ensuring that the obtained MBUs were induced by the same particle is important. The experiment was divided into many runs, and each experiment run should be short to maintain a low number of upsets because the number of coincident single-event upsets (CSEUs), which are caused by accumulating SEUs in FPGAs before reading back, will be reduced. Estimating the probability of the CSEU which may affect data accuracy is important. The probability of coincident SBUs in the readback file with the function of the matrix size and the number of upsets in the readback is calculated as Eq. (1) [10].

$$Prob_k(n,p)(collision) \approx 1 - e^{\frac{-p(p-1)(2k-1)}{2n}}, \quad (1)$$

In this equation, n is the number of bits in the DUT, and there are 24,071,936 bits for XC7K70T, p is the average number of upsets in each readback, k is the "collision range", which can be understood as the minimum number of bits separating the errors induced by the random event. And there are 3232 bits in a frame, considering the definition of MBU, the collision range should not beyond 3232. In order to improve the accuracy, the collision range was set to 808, which corresponds to a quarter of a frame [13]. And the credibility has been verified by the Monte Carlo method [11,12].

4. Results and discussions

The Xilinx Kintex-7 FPGA, XC7K70T, was tested under the protons, and the results are presented in the next paragraph.

4.1. Low-energy proton experimental results

SEUs on FPGA under the low-energy protons were obtained by comparing the bitstreams in the DUT and the golden. Fig. 4 shows the SEU cross sections for XC7K70T at room temperature. It can be seen that the SEU cross sections for 28 nm FPGA reached their peak when 5 MeV protons passed through 124 μm aluminum foil, meanwhile, the proton energy at interface of the DUT was 2.66 MeV. In Table 1, when 5 MeV proton passed through 100 μm aluminum foil, the range in silicon of the incident proton is 102.91 μm. When the thickness of aluminum foil was greater than 100 μm, the cross section should keep low or even not if the substrate thickness was 100 μm after grinding. However, the range in silicon substrate corresponding to the SEU cross section peak is about 75.58 μm. Obviously, the true thickness of the substrate must be less than 100 μm which we set before. The LET of the protons passing through different thickness of aluminum foil varies with the depth of silicon are shown in Fig. 5. It should be noted that SEU cross section will be generated as the Brag Peak locating at the sensitive region [14]. Therefore, it can be inferred that the true thickness of the substrates after thinning was approximately 75 μm.

Fig. 6 shows that the LET of protons in silicon varies with the proton energy calculated via SRIM2008. And from reference [13] we can know

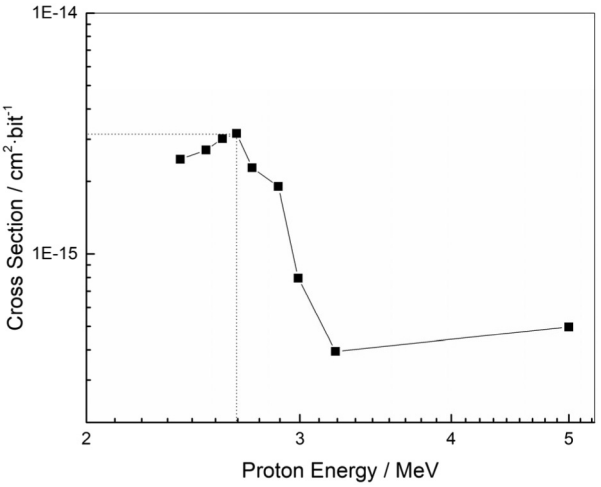

Fig. 4. SEU cross section of configuration memory on XC7K70T under low energy proton test.

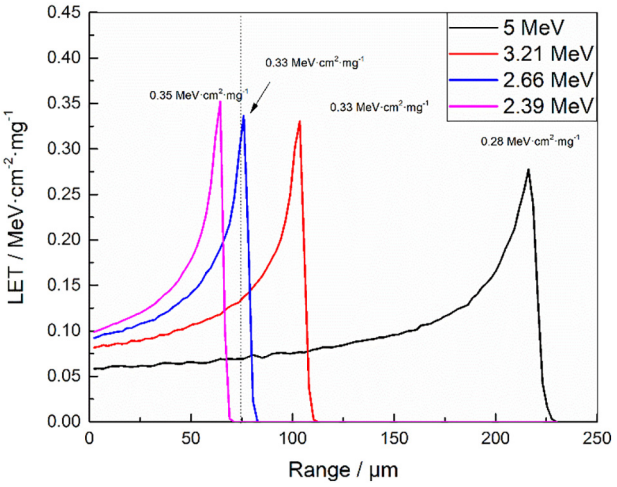

Fig. 5. Proton LET corresponding to the penetration depth after 5 MeV penetrating through Al foils of different thickness.

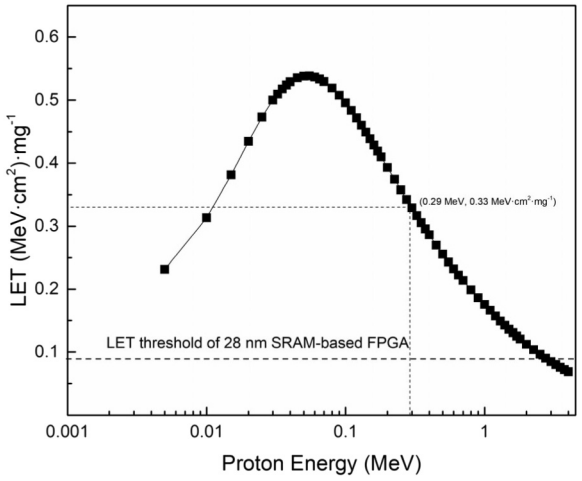

Fig. 6. The LET of low energy proton calculated by SRIM.

that the LET threshold of 28 nm SRAM-based FPGA is less than 0.1 MeV·cm^2·mg^{-1}. It can be seen that when the proton energy in sensitive regions was less than 1 MeV, the corresponding LET were all higher than the threshold. It should be noted that the LET corresponding to 2.66 MeV proton was low, which may not cause SEUs. However, after 2.66 MeV proton passed through the silicon substrates, the average energy located at the sensitive region was around 0.29 MeV, at this point, the corresponding LET was around 0.33 MeV·cm^2·mg^{-1}, and it was higher than 0.1 MeV·cm^2·mg^{-1}. This can cause the SEU, and SEU cross section peak could be generated. It can be sure that the SEU under the low-energy proton experiments are induced by direct ionization. Also, the energy spectrum broadening is evident after the proton passed through the degraders, and the energy of protons that have reached the sensitive region diverges, that's why the gaps of the cross sections near the peak are very small. However, there was about 75 μm silicon substrate, when the proton energy was lower than 2.66 MeV, the number of protons reaching the sensitive region was less, and the corresponding cross section was lower than the peak. Moreover, when the proton energy was higher than 2.66 MeV, the range of the proton was beyond the thickness of the substrate, then the proportion of the protons whose Brag Peak located at the sensitive region is decreasing with the energy rising.

Fig. 7 shows the configuration memory MBU cross section of XC7K70T. Four results of the low energy proton tests were selected to evaluate the MBU. Table 2 lists the details of the readback data from the

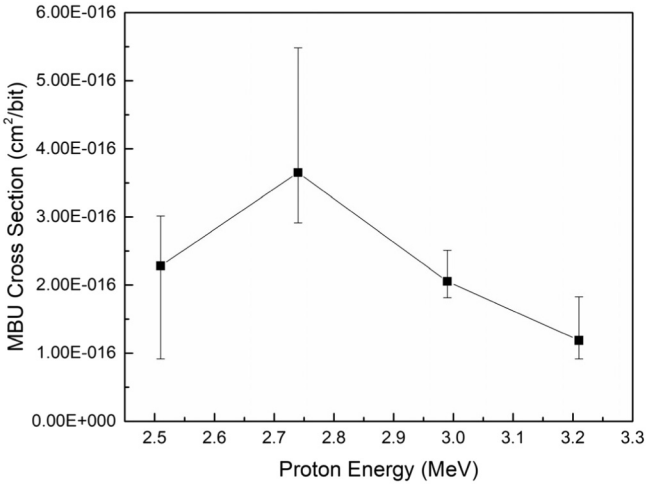

Fig. 7. MBU cross section of XC7K70T under the low-energy proton test.

Table 2
Readback-data under low-energy protons.

Run	Proton energy (MeV)	Total upsets	Upset bits Average upsets per readback (percentage of total bits)	$Prob_k(n,p)$ (collision)
1	2.51	188	3.84 (1.59E−5)	0.037%
2	2.74	164	4.32 (1.79E−5)	0.048%
3	2.99	617	30.85 (1.28E−4)	3.041%
4	3.21	102	6 (2.49E−5)	0.101%

DUT under the selected protons. Differences exist in the readbacks of different runs because of the dissimilarities in the flux rate and the irradiation times.

Reference [12] emphasized that CSEU will have less probability when the device had few SEUs in each run. The readbacks under the protons were minimal, and the probability of a CSEU, which is calculated with Eq. (1), is also shown in Table 2. The probability of CSEUs in this experiment is less than 3.1%, indicating that the "MBUs" in each run can be considered as true MBUs. It can be seen that a peak exists in the MBU cross section under the low-energy protons. And the MBU cross section was only one order of magnitude lower than SEU cross section. The results indicated that MBUs under the low-energy protons had become more obvious on FPGA with small feature size.

4.2. High-energy proton experimental results

Fig. 8 depicts the SEU cross section of the configuration memory irradiated by 50 and 90 MeV protons. The cross sections were slowly increased and were close to the saturation. The cross sections of BRAM were also illustrated in Fig. 8. The cross section we obtained is similar to the published paper which proves our results are credible [5].

The differences of the SEU cross sections in configuration memory and BRAM were clear. It can be seen that SEU cross section of BRAM was an order of magnitude lower than the configuration memory cross section. These differences proved that the sensitivity of resources in FPGA was indeed different. And the results of high-energy proton experiment may also reveal that the technology of BRAM was different from configuration memory in XC7K70T.

The results of the high energy proton test were compared with those of its low-energy counterpart. Low-energy protons have high LET values. The comparison of Fig. 4 with Fig. 8 shows that the SEU cross section located at the peak and the SEU cross section that calculated under the high-energy protons were on the same order of magnitude. The results indicate that SEU on FPGA induced by low energy protons

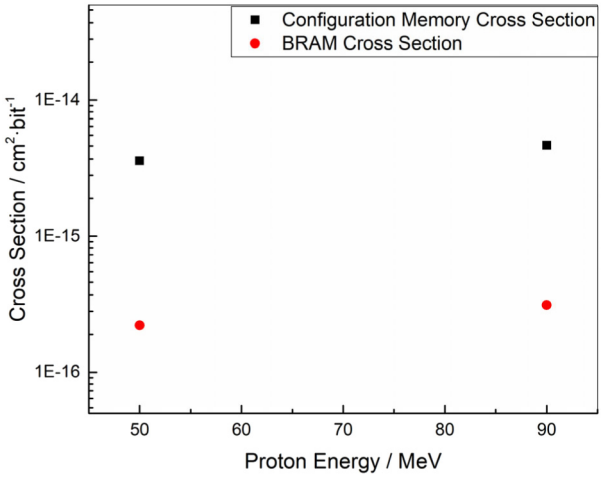

Fig. 8. The SEU characters of XC7K70T under high energy proton test.

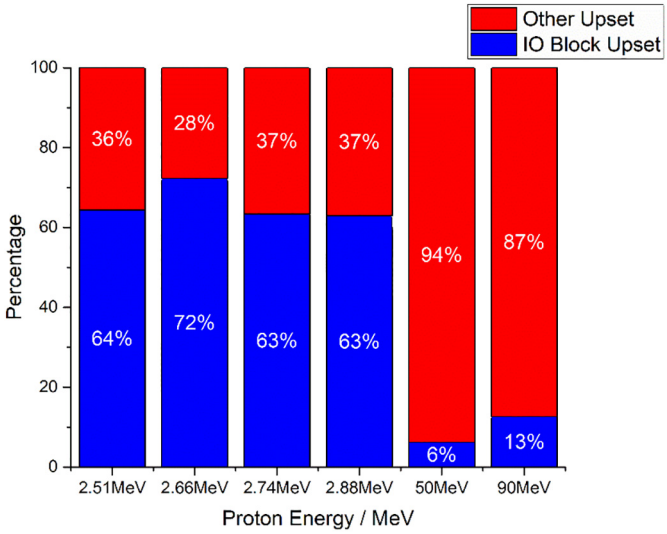

Fig. 9. The upset number of the frames related to IOB compared with the upset number in other frames.

can no longer be ignored.

Indeed, there are also something interesting in the experiment. It should be admitted that we inferred the corresponding frames for each resource roughly because of the complexity of current FPGAs, and the bitstream just can be divided into the frames related to CLB, DSP, CLK, IOB and BRAM, all of them are composed of their own control bits and the corresponding interconnected resources control bits. Therefore, the resources, such as CLB, BRAM, DSP and IOB, were bundled with the corresponding interconnected resources around them to analyze the phenomenon of the experiment. Actually the proportion of the frames related to the IOB is about 10%, normally the proportion of the upset frames related to the IOB should be near to 10%. However, we did find that a high proportion of the flipped frames related to IOB in the low-energy proton experiment but a normal percentage was obtained in the high-energy proton experiment which is shown in Fig. 9. And the result is actually consistent with the research [15]. Analysis of the data shows that the upsets of the high-energy proton are relatively balanced in the distribution of various resources, and the upsets of the BRAM were not be observed in the low-energy proton experiment. We infer that the LET thresholds in the BRAM and IOB are different. In other words, the LET thresholds in IOB and the interconnected resources are lower than which in BRAMs. Also, the upsets in the frames related to IOB were more than any other resources in the low-energy proton experiment, which means IOB is more sensitive than other resources. Given that the sensitivity of BRAM is different from the configuration memory, which is a strong probability that the structure of BRAM is different from the configuration memory. And the experimental results indicate that the LET threshold of BRAM is higher than others.

5. Conclusions

In this work, a self-developed 28 nm FPGA SEU test system was developed, and the XC7K70T, which is part of Kintex-7 FPGA family, was selected to test with protons under proton cyclotron accelerator (CIAE) and EN tandem accelerator in the Peking University. This work highlights the impact of the low energy proton on 28 nm FPGA.

The SEU and MBU cross sections induced by low energy protons were presented. The LET threshold for 28 nm FPGA was lower than 0.1 MeV·cm^2·mg^{-1}. Moreover, the very serious effect of low-energy protons on SEUs of 28 nm FPGAs was depicted by comparing the experimental results with those tested under high-energy protons which were on the same order of magnitude. Thereby indicating that the SEE characters of low-energy protons on small-feature-size FPGA must be considered.

Furthermore, we found the BRAM cross sections obtained from high-energy proton experiment were different from the configuration memory cross sections. What's more, the upsets in BRAM was not observed in low-energy proton experiments, however, the proportion of upsets in the frames related to IOB were much higher, which further proved that resources in FPGA have different LET threshold. We suggest that more attention and reinforcement should be paid on the IOB resources. It's true that this complexity will be a challenge for hardening FPGA.

CRediT authorship contribution statement

Zibo Wang: Data curation, Writing - original draft. **Wei Chen:** Supervision. **Zhibin Yao:** Software, Conceptualization. **Fengqi Zhang:** Investigation. **Yinhong Luo:** Formal analysis. **Xiaobin Tang:** Writing - review & editing. **Xiaoqiang Guo:** Visualization. **Lili Ding:** Methodology. **Cong Peng:** Investigation.

Declaration of competing interest

The authors declared that they have no conflicts of interest to this work.

We declare that we do not have any commercial or associative interest that represents a conflict of interest in connection with the work submitted.

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